MOTOROLA

Professional Radio

GM Series

VHF (136-174MHz)

Service Information

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Table of Contents

Chapter 1 MODEL CHART AND TECHNICAL SPECIFICATIONS

Chapter 2 THEORY OF OPERATION

Chapter 3 TROUBLESHOOTING CHARTS

Chapter 4 VHF PCB/SCHEMATICS/PARTS LISTS

Chapter 1

MODEL CHART AND TECHNICAL SPECIFICATIONS

1.0 GM140/GM160 Model Chart

GM Series VHF 136-174 MHz			
Model			Description
MDM25KKC9AA1_E			GM140, 136-174 MHz, 25-45W, 4 Ch
	MDM25KKF9AA5_E		GM160, 136-174 MHz, 25-45W, 128 Ch
		Item	Description
X		GCN6112_	Control Head, GM140
	X	GCN6114_	Control Head, GM160
X		IMUD6015_S	Field Replaceable Unit (Main Board) GM140
	X	IMUD6015_S	Field Replaceable Unit (Main Board) GM160
X	X	ENBN4056_	Packaging, Waris Mobile Radio
X	X	GLN7324_	Low Profile Mounting Trunnion
X	X	HKN9402_	12V Power Cable, 25-45W
X	X	MDRMN4025_	Enhanced Compact Microphone
X		6864110B86	User Guide, GM140
	X	6864110B87	User Guide, GM160
X = Indicates one of each is required			

2.0 GM340/GM360/GM380 Model Chart

GM Series VHF 136-174 MHz				
Model				Description
MDM25KHC9AN1_E				GM340, 136-174 MHz, 1-25W, 6 Ch
	MDM25KHF9AN5_E			GM360, 136-174 MHz, 1-25W, 255 Ch
		MDM25KHN9AN8_E		GM380, 136-174 MHz, 1-25W, 255 Ch
			Item	**Description**
X			GCN6112_	Control Head GM340
	X		GCN6120_	Control Head GM360
		X	GCN6121_	Control Head GM380
X			IMUD6013_S	Field Replaceable Unit (Main Board) GM340
	X		IMUD6013_S	Field Replaceable Unit (Main Board) GM360
		X	IMUD6024_S	Field Replaceable Unit (Main Board) GM380
X	X	X	ENBN4056_	Packaging, Waris Mobile
X	X	X	GLN7324_	Low Profile Mounting Trunnion
X	X	X	HKN4137_	12V Power Cable 1-25W
X	X	X	MDRMN4025_	Enhanced Compact Microphone
X			6864110B80	User Guide GM340
	X		6864110B81	User Guide, GM360
		X	6864110B82	User Guide, GM380
X = Indicates one of each is required				

3.0 GM640/GM660/GM1280 Model Chart

GM Series VHF 136-174 MHz				
Model				Description
MDM25KHC9CK1_E				GM640, 136-174 MHz, 1-25W, 6 Ch
	MDM25KHF9CK5_E			GM660, 136-174 MHz, 1-25W, 255 Ch
		MDM25KHN9CK8_E		GM1280, 136-174 MHz, 1-25W, 255 Ch
			Item	**Description**
X			GCN6112_	Control Head GM640
	X		GCN6120_	Control Head GM660
		X	GCN6121_	Control Head GM1280
X			IMUD6018_S	Field Replaceable Unit (Main Board) GM640
	X		IMUD6018_S	Field Replaceable Unit (Main Board) GM660
		X	IMUD6018_S	Field Replaceable Unit (Main Board) GM1280
X	X	X	ENBN4056_	Packaging, Waris Mobile Radio
X	X	X	GLN7324_	Low Profile Mounting Trunnion
X	X	X	HKN4137_	12V Power Cable, 1-25W
X	X	X	MDRMN4025_	Enhanced Compact Microphone
X			6864110B83_	User Guide, GM640
	X		6864110B84_	User Guide, GM660
		X	6864110B85_	User Guide, GM1280

X = Indicates one of each is required.

4.0 Technical Specifications

Data is specified for +25°C unless otherwise stated.

General Specifications	
Channel Capacity **GM140** **GM160** **GM340** **GM360** **GM380** **GM640** **GM660** **GM1280**	 4 128 6 255 255 6 255 255
Power Supply	13.2Vdc (10.8 - 15.6Vdc)
Dimensions: H x W x D (mm) Depth excluding knobs	**GM140/340/640** 56mm x 176mm x 177mm (1 - 25W) 56mm x 176mm x 189mm (25 - 45W) (add 8mm for Volume Knob)
Dimensions: H x W x D (mm) Depth excluding knobs	**GM160/360/660** 59mm x 179mm x 186mm (1 - 25W) 59mm x 179mm x 198mm (25 - 45W) (add 9mm for Volume Knob)
Dimensions: H x W x D (mm) Depth excluding knobs	**GM380/1280** 188mm x 185mm x 72mm (add 8mm for Volume Knob)
Weight **GM140/340/640**	1400gr
Weight **GM160/360/660**	1400gr
Weight **GM380/1280**	1500gr
Sealing:	Withstands rain testing per MIL STD 810 C/D /E and IP54
Shock and Vibration:	Protection provided via impact resistant housing exceeding MIL STD 810-C/D /E and TIA/EIA 603
Dust and Humidity:	Protection provided via environment resistant housing exceeding MIL STD 810 C/D /E and TIA/EIA 603

Transmitter	VHF
*Frequencies - Full Bandsplit	VHF 136-174 MHz
Channel Spacing	12.5/20/25 kHz
Frequency Stability (-30°C to +60°C, +25° Ref.)	±2.5 ppm
Power	1-25W / 25-45W
Modulation Limiting	±2.5 @ 12.5 kHz ±4.0 @ 20 kHz ±5.0 @ 25 kHz
FM Hum & Noise	-40 dB @ 12.5kHz -45 dB @ 20/25kHz
Conducted/Radiated Emission (ETS)	-36 dBm <1 GHz -30 dBm >1 GHz
Adjacent Channel Power	-60 dB @ 12.5 kHz -70 dB @ 25 kHz
Audio Response (300 - 3000Hz)	+1 to -3 dB
Audio Distortion @1000Hz, 60% Rated Maximum Deviation	<3% typical

Receiver	VHF
*Frequencies - Full Bandsplit	VHF 136-174 MHz
Channel Spacing	12.5/20/25 kHz
Sensitivity (12 dB SINAD)	0.30 µV (0.22 µV typical)
Intermodulation (ETS)	>65 dB Base Mode: >70dB (1-25W model only)
Adjacent Channel Selectivity (ETS)	65 dB @ 12.5 kHz 75 dB @ 20 kHz 80 dB @ 25 kHz
Spurious Rejection (ETS)	75 dB @ 12.5 kHz 80 dB @ 20/25 kHz
Rated Audio	3W Internal 13W External
Audio Distortion @ Rated Audio	<3% typical
Hum & Noise	-40 dB @ 12.5 kHz -45 dB @ 20/25 kHz
Audio Response (300 - 3000Hz @ 20/25kHz) (300 - 2550Hz @12.5kHz)	+1 to -3 dB
Conducted Spurious Emission (ETS)	-57 dBm <1 GHz -47 dBm >1 GHz

*Availability subject to the laws and regulations of individual countries.

Chapter 2

THEORY OF OPERATION

1.0 Introduction

This Chapter provides a detailed theory of operation for the VHF circuits in the radio. For details of the theory of operation and trouble shooting for the the associated Controller circuits refer to the Controller Section of this manual.

2.0 VHF (136-174MHz) Receiver

2.1 Receiver Front-End

The receiver is able to cover the VHF range from 136 to 174 MHz. It consists of four major blocks: front-end bandpass filters and pre-amplifier, first mixer, high-IF, low-IF and receiver back-end. Two varactor-tuned bandpass filters perform antenna signal pre-selection. A cross over quad diode mixer converts the signal to the first IF of 44.85 MHz. High-side first injection is used.

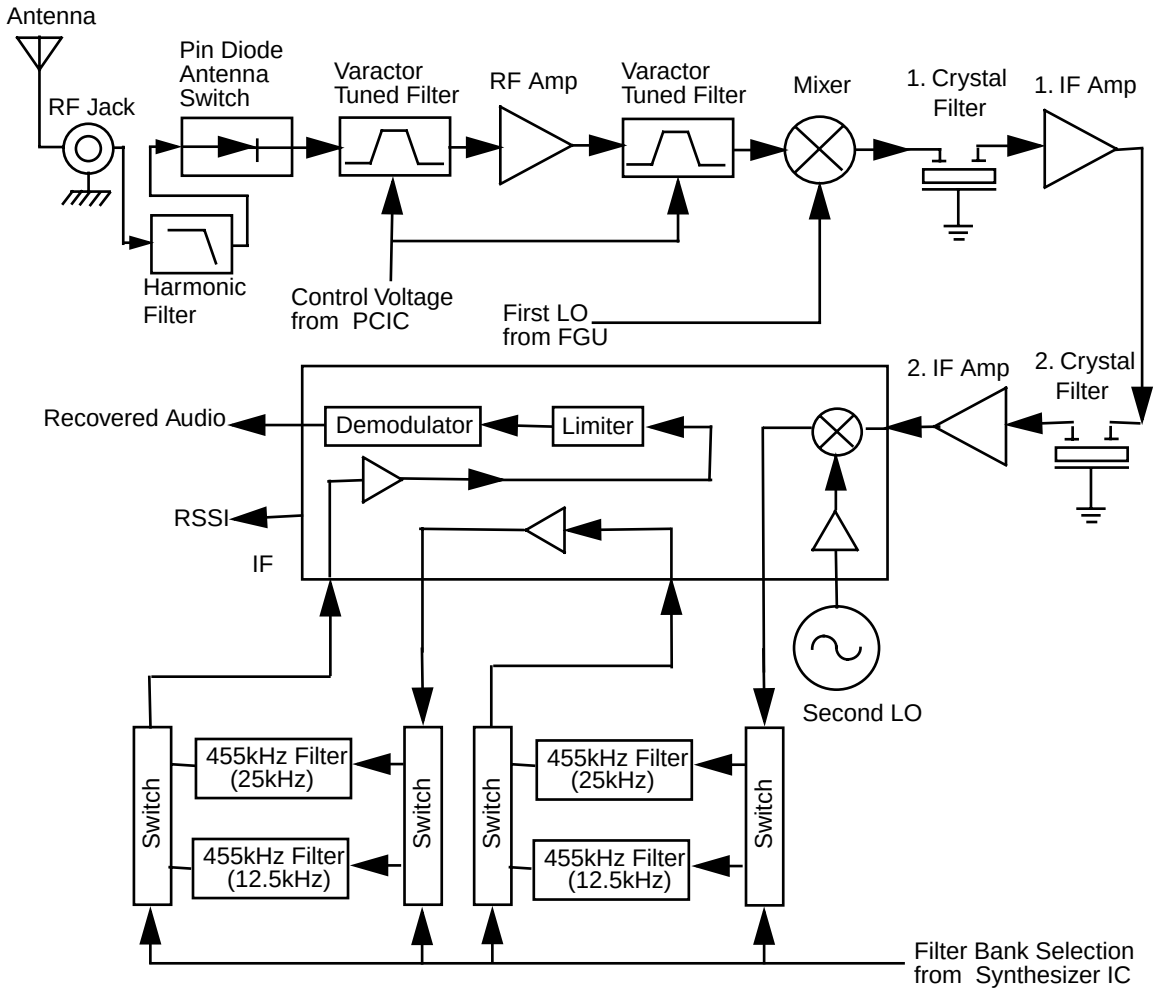


Figure 2-1 VHF Receiver Block Diagram

There are two 2-pole 44.85 MHz crystal filters in the high-IF section and 2 pairs of 455 kHz ceramic filters in the low-IF section to provide the required adjacent channel selectivity. The correct pair of ceramic filters for 12.5 or 25kHz channel spacing is selected via control line BWSELECT. The second IF at 455 kHz is mixed, amplified and demodulated in the IF IC. The processing of the demodulated audio signal is performed by an audio processing IC located in the controller section.

2.2 Front-End Band-Pass Filters & Pre-Amplifier

The received signal from the radio's antenna connector is first routed through the harmonic filter and antenna switch, which are part of the RF power amplifier circuitry, before being applied to the receiver pre-selector filter (C3001, C3002, D3001 and associated components). The 2-pole pre-selector filter tuned by the dual varactor diode D3001 pre-selects the incoming signal (RXIN) from the antenna switch to reduce spurious effects to following stages. The tuning voltage (FECNTL_1) ranging from 2 volts to 8 volts is controlled by pin 20 of PCIC (U3501) in the Transmitter section. A dual hot carrier diode (D3003) limits any inband signal to 0 dBm to prevent damage to the pre-amplifier.

The RF pre-amplifier is an SMD device (Q3001) with collector-base feedback to stabilize gain, impedance, and intermodulation. Transistor Q3002 compares the voltage drop across resistor R3002 with a fixed base voltage from divider R3011, R3000 and R3012, and adjusts the base current of Q3001 as necessary to maintain its collector current constant at approximately 15-20 mA. Operating voltage is from the regulated 9.3V supply (9V3). During transmit, 9.1 volts (K9V1) turns off both transistors Q3002 and Q3001. This protects the RF pre-amplifier from excessive dissipation during transmit mode. A switchable 3dB pad (R3022, R3024, R3016 and R3018) controlled via Line FECNTL_2 and Q3021 stabilizes the output impedance and intermodulation performance.

A second 2-pole varactor tuned bandpass filter provides additional filtering of the amplified signal. The dual varactor diode D3004 is controlled by the same signal FECNTL_1, which controls the pre-selector filter.

2.3 First Mixer and High Intermediate Frequency (IF)

The signal coming from the front-end is converted to the high-IF frequency of 44.85 MHz using a cross over quad diode mixer (D3031). Its ports are matched for incoming RF signal conversion to the 44.85 MHz IF using high side injection. The high-side injection signal (RXINJ) from the frequency synthesizer circuitry has a level of approximately 13 dBm and is injected via matching transformer T3002.

The mixer IF output signal (IF) from transformer T3001 pin 2 is fed to the first two pole crystal filter FL3101. The filter output in turn is matched to the following IF amplifier.

The IF amplifier Q3101 is actively biased by a collector base feedback (R3101, R3106) to a current drain of approximately 5 mA drawn from the voltage 5V. Its output impedance is matched to the second two pole crystal filter FL3102. The signal is further amplified by a preamplifier (Q3102) before going into pin 1 of IFIC (U3101).

A dual hot carrier diode (D3101) limits the filter output voltage swing to reduce overdrive effects at RF input levels above -27 dBm.

2.4 Low Intermediate Frequency (IF) and Receiver Back End

The 44.85 MHz high-IF signal from the second IF amplifier feeds the IF IC (U3101) at pin1. Within the IF IC, the 44.85 MHz high IF signal mixes with the 44.395 MHz second local oscillator (2nd LO) to produce the low-IF signal at 455 kHz. The 2nd LO frequency is determined by crystal Y3101. The

low IF signal is amplified and filtered by an external pair of 455 kHz ceramic filters FL3112, FL3114 for 20/25 kHz channel spacing or FL3111, FL3113/F3115 for 12.5 kHz channel spacing. These pairs are selectable via BWSELECT. The filtered output from the ceramic filters is applied to the limiter input pin of the IF IC (pin 14).
The IF IC contains a quadrature detector using a ceramic phase-shift element (Y3102) to provide audio detection. Internal amplification provides an audio output level of 120 mV rms (at 60% deviation) from U3101 pin 8 (DISCAUDIO) which is fed to the ASFIC_CMP (U0221) pin 2 (part of the Controller circuitry).
A received signal strength indicator (RSSI) signal is available at U3101 pin 5, having a dynamic range of 70 dB. The RSSI signal is interpreted by the microprocessor (U0101 pin 63) and in addition is available at accessory connector J0501-15.

3.0 VHF (136-174MHz) Transmitter Power Amplifier (PA) 25 W

The radio's 25 W PA is a three stage amplifier used to amplify the output from the VCOBIC to the radio transmit level. All three stages utilize LDMOS technology. The gain of the first stage (U3401) and the second stage (Q3421) is adjustable, controlled by pin 4 of PCIC (U3501) via U3402-1 and U3402-2. It is followed by an LDMOS final stage (Q3441).

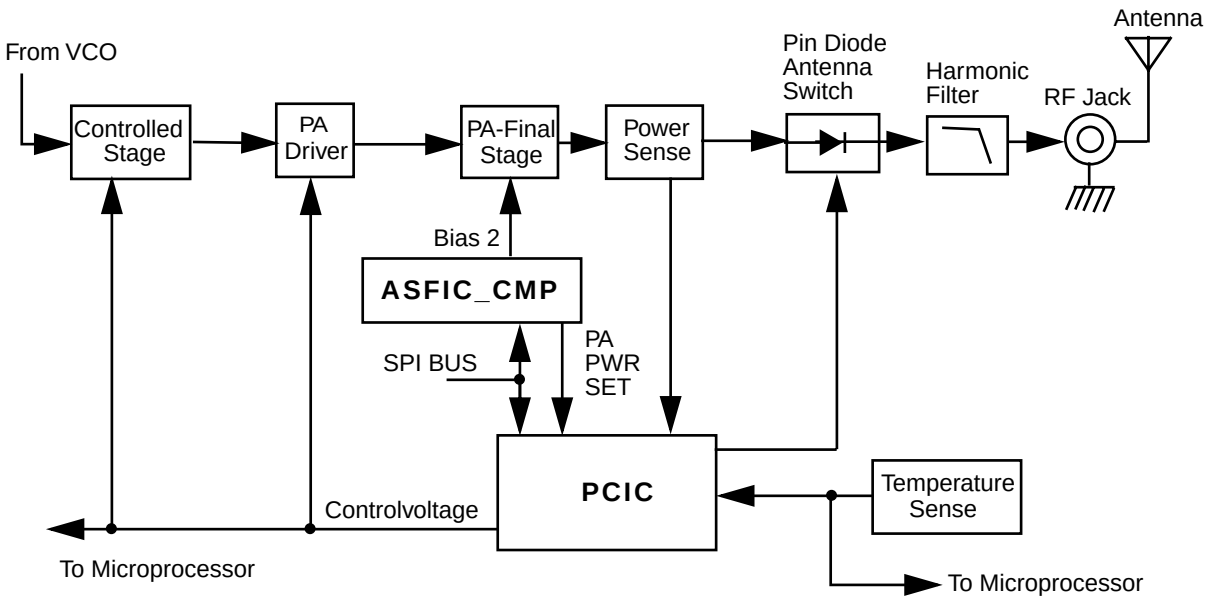


Figure 2-1 VHF Transmitter Block Diagram

Devices U3401, Q3421 and Q3441 are surface mounted. A pressure pad between board and the radio's cover provides good thermal contact between the devices and the chassis.

3.1 First Power Controlled Stage

The first stage (U3401) is a 20dB gain integrated circuit containing two LDMOS FET amplifier stages. It amplifies the RF signal from the VCO (TXINJ). The output power of stage U3401 is controlled by a DC voltage applied to pin 1 from the op-amp U3402-1, pin 1. The control voltage simultaneously varies the bias of two FET stages within U3401. This biasing point determines the overall gain of U3401 and therefore its output drive level to Q3421, which in turn controls the output power of the PA.

Op-amp U3402-1 monitors the drain current of U3401 via resistor R3444 and adjusts the bias voltage of U3401 so that the current remains constant. The PCIC (U3501) provides a DC output voltage at pin 4 (INT) which sets the reference voltage of the current control loop. A raising power output causes the DC voltage from the PCIC to fall, and U3402-1 adjusts the bias voltage for a lower drain current to lower the gain of the stage.
In receive mode the DC voltage from PCIC pin 23 (RX) turns on Q3442, which in turn switches off the biasing voltage to U3401.
Switch S3440 is a pressure pad with a conductive strip which connects two conductive areas on the board when the radio's cover is properly screwed to the chassis. When the cover is removed, S3440 opens and the resulting high voltage level at the inverting inputs of the current control op-amps U3402-1 & 2 switches off the biasing of U3401 and Q3421. This prevents transmitter key up while the devices do not have proper thermal contact to the chassis.

3.2 Power Controlled Driver Stage

The next stage is an LDMOS device (Q3421) providing a gain of 12dB. This device requires a positive gate bias and a quiescent current flow for proper operation. The bias is set during transmit mode by the drain current control op-amp U3402-2, and fed to the gate of Q3421 via the resistive network R3429, R3418, R3415 and R3416.

Op-amp U3402-2 monitors the drain current of U3421 via resistors R3424-27 and adjusts the bias voltage of Q3421 so that the current remains constant. The PCIC (U3501) provides a DC output voltage at pin 4 (INT) which sets the reference voltage of the current control loop. A raising power output causes the DC voltage from the PCIC to fall, and U3402-2 adjusts the bias voltage for a lower drain current to lower the gain of the stage.
In receive mode the DC voltage from PCIC pin 23 (RX) turns on Q3422, which in turn switches off the biasing voltage to Q3421.

3.3 Final Stage

The final stage is an LDMOS device (Q3441) providing a gain of 12dB. This device also requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line MOSBIAS_2 is set in transmit mode by the ASFIC and fed to the gate of Q3441 via the resistive network R3404, R3406, and R3431-5. This bias voltage is tuned in the factory. If the transistor is replaced, the bias voltage must be tuned using the Customer Programming Software (CPS). Care must be taken not to damage the device by exceeding the maximum allowed bias voltage. In receive mode U3402-2 pulls the bias voltage to low via D3401. The device’s drain current is drawn directly from the radio’s DC supply voltage input, PASUPVLTG, via L3436 and L3437.
A matching network consisting of C3441-49, L3443, and two striplines, transforms the impedance to 50 ohms and feeds the directional coupler.

3.4 Directional Coupler

The directional coupler is a microstrip printed circuit, which couples a small amount of the forward power delivered by Q3441. The coupled signal is rectified by D3451. The DC voltage is proportional to the RF output power and feeds the RFIN port of the PCIC (U3501 pin 1). The PCIC controls the gain of stage U3401 and Q3421 as necessary to hold this voltage constant, thus ensuring the forward power out of the radio to be held to a constant value.

3.5 Antenna Switch

The antenna switch consists of two PIN diodes, D3471 and D3472. In the receive mode, both diodes are off. Signals applied at the antenna jack J3401 are routed, via the harmonic filter, through network L3472, C3474 and C3475, to the receiver input. In the transmit mode, K9V1 turns on Q3471 which enables current sink Q3472, set to 96 mA by R3473 and VR3471. This completes a DC path from PASUPVLTG, through L3437, D3471, L3472, D3472, L3471, R3474 and the current sink, to ground. Both diodes are forward biased into conduction. The transmitter RF from the directional coupler is routed via D3471 to the harmonic filter and antenna jack. D3472 also conducts, shunting RF power and preventing it from reaching the receiver port (RXIN). L3472 is selected to appear as a lambda / 4 wave transmission line, making the short circuit presented by D3472 appear as an open circuit at the junction of D3472 and the receiver path.

3.6 Harmonic Filter

Components L3491-L3493 and L3472, C3491-C3499 form a Chebychev low-pass filter to attenuate harmonic energy of the transmitter to specifications level. R3491 is used to drain electrostatic charge that might otherwise build up on the antenna. The harmonic filter also prevents high level RF signals above the receiver passband from reaching the receiver circuits, improving spurious response rejection.

3.7 Power Control

The transmitter uses the Power Control IC (PCIC, U3501) to control the power output of the radio. A portion of the forward RF power from the transmitter is sampled by the directional coupler and rectified, to provide a DC voltage to the RFIN port of the PCIC (pin 1) which is proportional to the sampled RF power.
The ASFIC (U0221) has internal digital to analog converters (DACs) which provide a reference voltage of the control loop to the PCIC via R3505. The reference voltage level is programmable through the SPI line of the PCIC. This reference voltage is proportional to the desired power setting of the transmitter, and is factory programmed at several points across the frequency range of the transmitter to offset frequency response variations of the transmitter's power detector circuit.
The PCIC provides a DC output voltage at pin 4 (INT) which sets the drain current of the first (U3401) and second (Q3421) transmitter stage via current control op-amps U3402-1 and U3402-2. This adjusts the transmitter power output to the intended value. Variations in forward transmitter power cause the DC voltage at pin 1 to change, and the PCIC adjusts the control voltage above or below its nominal value to raise or lower output power. Capacitors C3502-4, in conjunction with resistors and integrators within the PCIC, control the transmitter power-rise (key-up) and power-decay (de-key) characteristic to minimize splatter into adjacent channels. U3502 is a temperature-sensing device, which monitors the circuit board temperature in the vicinity of the transmitter driver and final devices, and provides a dc voltage to the PCIC (TEMP, pin 30) proportional to temperature. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

4.0 VHF (136-174MHz) Frequency Synthesis

The frequency synthesizer subsystem consists of the reference oscillator (Y3261 or Y3263), the Low Voltage Fractional-N synthesizer (LVFRAC-N, U3201), and the voltage-controlled oscillators and buffer amplifiers (U3301, Q3301-2 and associated circuitry).

4.1 Reference Oscillator

The reference oscillator (Y3263) contains a temperature compensated crystal oscillator with a frequency of 16.8 MHz. An analog to digital (A/D) converter internal to U3201 (LVFRAC-N) and controlled by the microprocessor via serial interface (SRL) sets the voltage at the warp output of U3201 (pin 25) to set the frequency of the oscillator. The output of the oscillator (U3263 pin 3) is applied to pin 23 (XTAL1) of U3201 via R3263 and C3235.

In applications were less frequency stability is required, the oscillator inside U3201 is used along with an external crystal Y3261, varactor diode D3261, C3261, C3262 and R3262. In this case, Y3263, R3263, C3235 and C3251 are not used. When Y3263 is used, Y3261, D3261, C3261, C3262 and R3262 are not used, and C3263 is increased to 0.1 uF.

4.2 Fractional-N Synthesizer

The LVFRAC-N synthesizer IC (U3201) consists of a pre-scaler, a programmable loop divider, control divider logic, a phase detector, a charge pump, an A/D converter for low frequency digital modulation, a balance attenuator to balance the high frequency analog modulation and low frequency digital modulation, a 13V positive voltage multiplier, a serial interface for control, and finally a super filter for the regulated 5 volts.

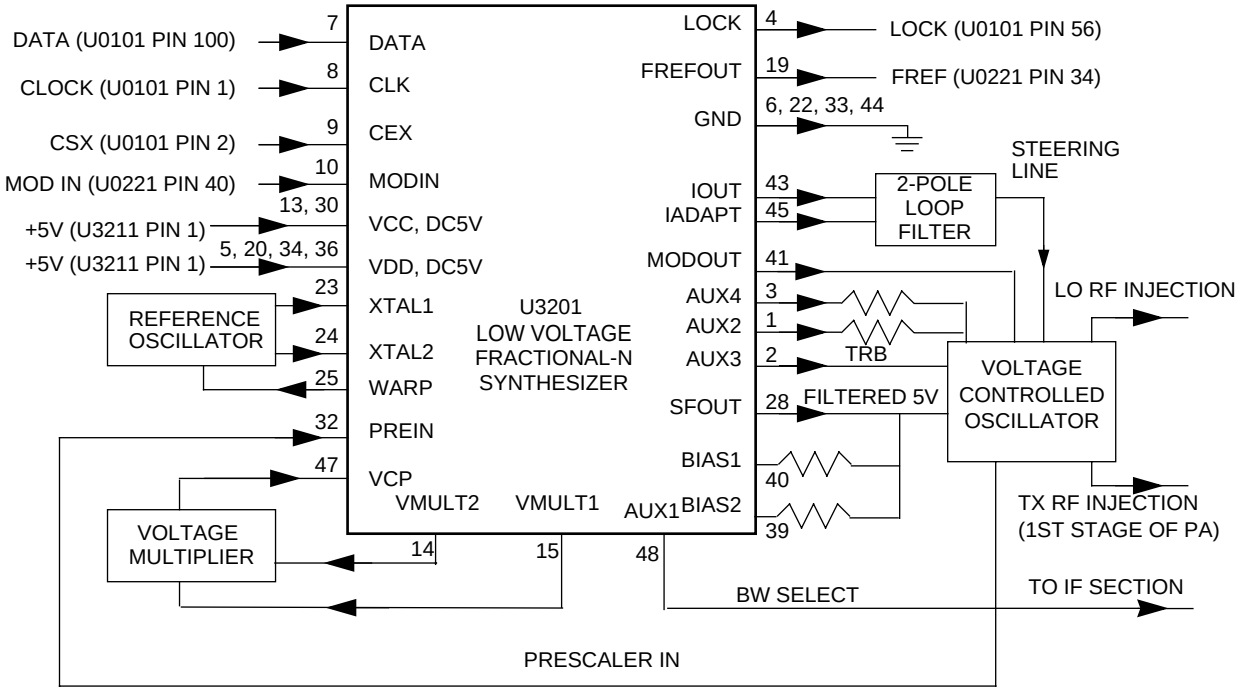


Figure 2-1 VHF Synthesizer Block Diagram

A voltage of 5V applied to the super filter input (U3201 pin 30) supplies an output voltage of 4.5 VDC (VSF) at pin 28. It supplies the VCO, VCO modulation bias circuit (via R3363) and the synthesizer charge pump resistor network (R3251, R3252). The synthesizer supply voltage is provided by the 5V regulator U3211.

In order to generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U3201-47), a voltage of 13 VDC is being generated by the positive voltage multiplier circuitry (D3201, C3202, C3203). This voltage multiplier is basically a diode capacitor network driven by two (1.05MHz) 180 degrees out of phase signals (U3201-14 and -15).

Output LOCK (U3201-4) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. IC U3201 provides the 16.8 MHz reference frequency at pin 19.

The serial interface (SRL) is connected to the microprocessor via the data line DATA (U3201-7), clock line CLK (U3201-8), and chip enable line CSX (U3201-9).

4.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) consists of the VCO/Buffer IC (VCOBIC, U3301), the TX and RX tank circuits, the external RX buffer stages, and the modulation circuitry.

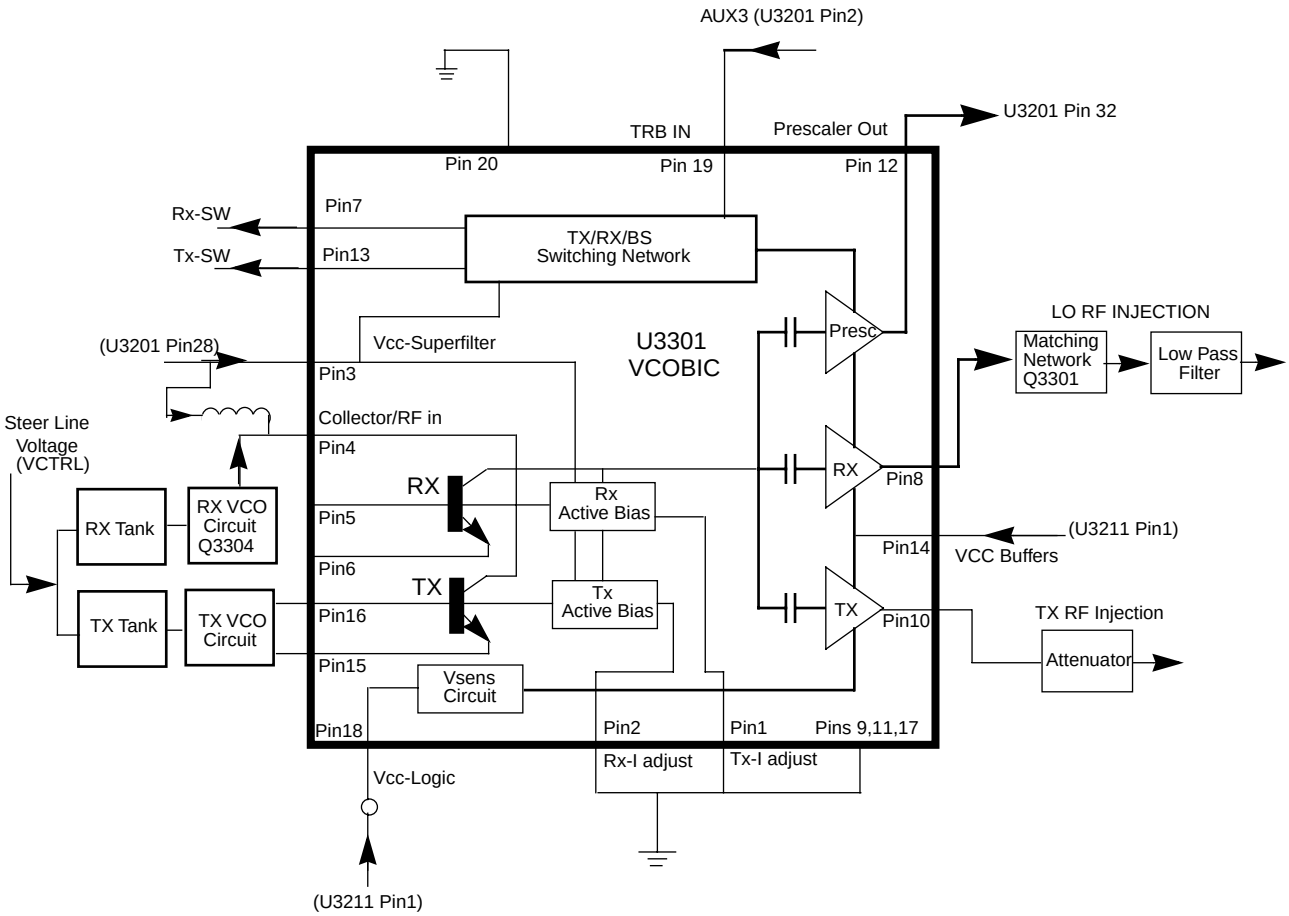


Figure 2-1 VHF VCO Block Diagram

The VCOBIC together with the Fractional-N synthesizer (U3201) generates the required frequencies in both the transmit and receive modes. The TRB line (U3301 pin 19) determines which tank circuits and internal buffers are to be enabled. A high level on TRB enables the TX tank and TX output (pin 10), and a low enables the RX tank and RX output (pin 8). A sample of the signal from the enabled RF output is routed from U3301 pin 12 (PRESC_OUT), via a low pass filter, to pin 32 of U3201 (PREIN).

A steering line voltage (VCTRL) between 2.5V and 11V at varactor diode D3361 will tune the full TX frequency range (TXINJ) from 136 MHz to 174 MHz, and at varactor diode D3341 will tune the full RX frequency range (RXINJ) from 181 MHz to 219 MHz. The RX tank circuit uses a Hartley configuration for wider bandwidth. For the RX tank circuit, an external transistor Q3304 is used for better side-band noise.

The external RX buffers (Q3301 and Q3302) are enabled by a high at U3301 pin 7 (RX_SWITCH) via transistor switch Q3303. In the TX mode, the modulation signal (VCOMOD) from the LVFRAC-N synthesizer IC (U3201 pin 41) is applied to varactor diode D3362, which modulates the TX VCO frequency via capacitor C3362. Varactor D3362 is biased for linearity from VSF.

4.4 Synthesizer Operation

The complete synthesizer subsystem consists of the low voltage FRAC-N (LVFRACN), the reference oscillator (a crystal oscillator with temperature compensation), charge pump circuitry, loop filter circuitry and a DC supply. The output signal PRESC from the VCOBIC (U3301 pin 12) is fed to U3201 pin 32 (PREIN) via a low pass filter (C3318, L3318 and C3226) which attenuates harmonics and provides the correct level to close the synthesizer loop.

The pre-scaler in the synthesizer (U3201) is a dual modulus type with selectable divider ratios. The divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the SRL. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider´s output signal with the reference signal. The reference signal is generated by dividing down the signal of the reference oscillator (Y3261 or Y3263).

The output signal of the phase detector is a pulsed DC signal which is routed to the charge pump. The charge pump outputs a current at U3201 pin 43 (IOUT). The loop filter (which consists of R3221-R3223 and C3221-C3224) transforms this current into a voltage that is applied to the varactor diodes (D3361 for transmit, D3341 for receive) to alter the output frequency of the appropriate VCO. The current can be set to a value fixed within the LVFRAC-N IC, or to a value determined by the currents flowing into BIAS 1 (U3201-40) or BIAS 2 (U3201-39). The currents are set by the value of R3251 and R3252 respectively. The selection of the three different bias sources is done by software programming.

To reduce synthesizer lock time when new frequency data has been loaded into the synthesizer, the magnitude of the loop current is increased by enabling the IADAPT pin (U3201-45) for a certain software programmable time (adapt mode). The adapt mode timer is started by a low to high transient of the CSX line. When the synthesizer is within the lock range, the current is determined only by the resistors connected to BIAS 1 and BIAS 2, or by the internal current source. A settled synthesizer loop is indicated by a high level signal at U3201-4 (LOCK).

The LOCK signal is routed to one of the µP´s ADC inputs (U0101-56). From the measured voltage, the µP determines whether LOCK is active.

In order to modulate the PLL, the two spot modulation method is utilized. Via U3201 pin 10 (MODIN), the audio signal is applied to both the A/D converter (low frequency path) as well as the balance attenuator (high frequency path). The A/D converter changes the low frequency analog modulating

signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is present at the MODOUT port (U3201-41) and connected to the VCO modulation diode D3362 via R3364.

5.0 VHF (136-174MHz) Transmitter Power Amplifier (PA) 45 W

The radio's 45 W PA is a four stage amplifier used to amplify the output from the VCOBIC to the radio transmit level. The line-up consists of three stages which utilize LDMOS technology, followed by a final stage using a bipolar device. The gain of the first stage (U3401) is adjustable, controlled by pin 4 of PCIC (U3501) via Q3501 and Q3502 (VCONT). It is followed by an LDMOS pre-driver stage (Q3421), an LDMOS driver stage (Q3431) and a bipolar final stage (Q3441).

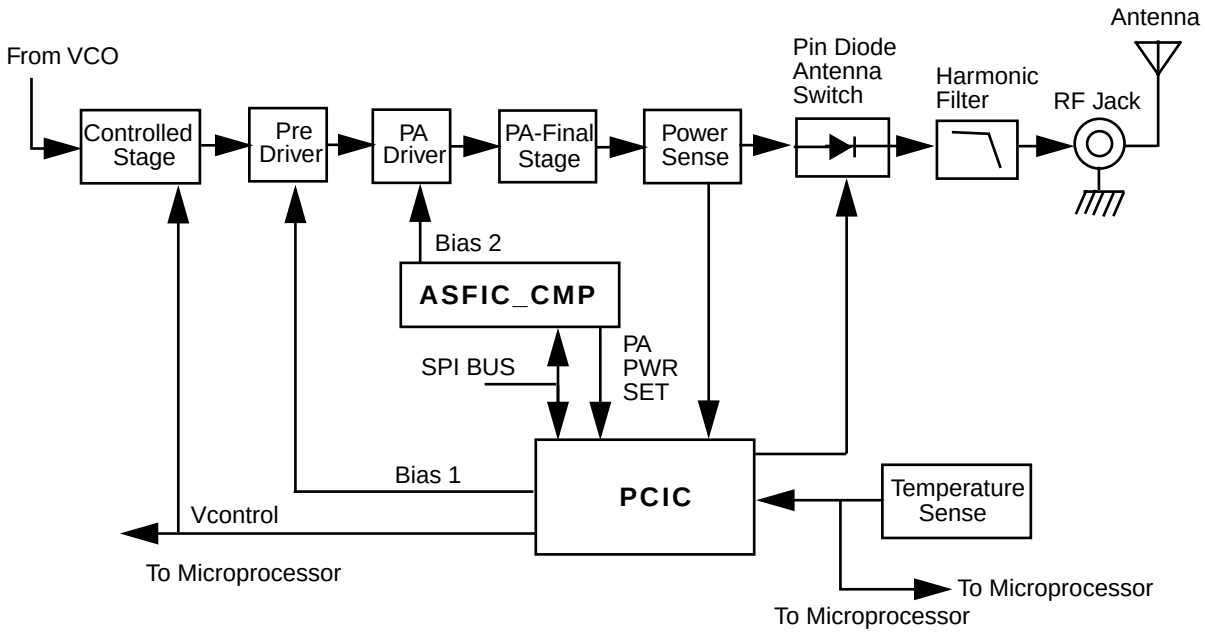


Figure 2-1 VHF Transmitter Block Diagram

Devices U3401 and Q3421 are surface mounted. The remaining devices are directly attached to the heat sink.

5.1 Power Controlled Stage

The first stage (U3401) is a 20dB gain integrated circuit containing two LDMOS FET amplifier stages. It amplifies the RF signal from the VCO (TXINJ). The output power of stage U3401 is controlled by a DC voltage applied to pin 1 from the power control circuit (U3501 pin 4, with transistors Q3501 and Q3502 providing current gain and level-shifting). The control voltage simultaneously varies the bias of two FET stages within U3401. This biasing point determines the overall gain of U3401 and therefore its output drive level to Q3421, which in turn controls the output power of the PA.

In receive mode the voltage control line is at ground level and turns off Q3501-2, which in turn switches off the biasing voltage to U3401.

5.2 Pre-Driver Stage

The next stage is an LDMOS device (Q3421) providing a gain of 13 dB. This device requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line PCIC_MOSBIAS_1 is set during transmit mode by the PCIC pin 24, and fed to the gate of Q3421 via the resistive network R3410, R3415, and R3416. The bias voltage is tuned in the factory.

5.3 Driver Stage

The following stage is an enhancement-mode N-Channel MOSFET device (Q3431) providing a gain of 10dB. This device also requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line MOSBIAS_2 is set in transmit mode by the ASFIC and fed to the gate of Q3431 via the resistive network R3404, R3406, and R3431-5. This bias voltage is also tuned in the factory. If the transistor is replaced, the bias voltage must be tuned using the Customer Programming Software (CPS). Care must be taken not to damage the device by exceeding the maximum allowed bias voltage. The device's drain current is drawn directly from the radio's DC supply voltage input, PASUPVLTG, via L3431 and L3432.

5.4 Final Stage

The final stage uses the bipolar device Q3441. The device's collector current is also drawn from the radio's DC supply voltage input. To maintain class C operation, the base is DC-grounded by a series inductor (L3441) and a bead (L3442). A matching network consisting of C3446-52, C3467, L3444-5, and two striplines, transforms the impedance to approximately 50 ohms and feeds the directional coupler.

5.5 Directional Coupler

The directional coupler is a microstrip printed circuit, which couples a small amount of the forward and reflected power delivered by Q3441. The coupled signals are rectified by D3451-2 and combined by R3463-4. The resulting DC voltage is proportional to RF output power and feeds the RFIN port of the PCIC (U3501 pin 1). The PCIC controls the gain of stage U3401 as necessary to hold this voltage constant, thus ensuring the forward power out of the radio to be held to a constant value.

An abnormally high reflected power level, such as may be caused by a damaged antenna, also causes the DC voltage applied to the PCIC to increase, and this will cause a reduction in the gain of U3401, reducing transmitter output power to prevent damage to the final device due to an improper load.

5.6 Antenna Switch

The antenna switch consists of two PIN diodes, D3471 and D3472. In the receive mode, both diodes are off. Signals applied at the antenna jack J3401 are routed, via the harmonic filter, through network L3472, C3474 and C3475, to the receiver input. In the transmit mode, K9V1 turns on Q3471 which enables current sink Q3472, set to 96 mA by R3473 and VR3471. This completes a DC path from PASUPVLTG, through L3473, D3471, L3477, L3472, D3472, L3471, R3474 and the current sink, to ground. Both diodes are forward biased into conduction. The transmitter RF from the directional coupler is routed via D3471 to the harmonic filter and antenna jack. D3472 also conducts, shunting RF power and preventing it from reaching the receiver port (RXIN). L3472 is selected to appear as a broadband lambda/4 wave transmission line, making the short circuit presented by D3472 appear as an open circuit at the junction of D3472 and the receiver path.

5.7 Harmonic Filter

Components L3491-L3494 and C3489-C3498 form a nine-pole Chebychev low-pass filter to attenuate harmonic energy of the transmitter to specifications level. R3490 is used to drain electrostatic charge that might otherwise build up on the antenna. The harmonic filter also prevents high level RF signals above the receiver passband from reaching the receiver circuits, improving spurious response rejection.

5.8 Power Control

The transmitter uses the Power Control IC (PCIC, U3501) to control the power output of the radio. A portion of the forward and reflected RF power from the transmitter is sampled by the directional coupler, rectified and summed, to provide a DC voltage to the RFIN port of the PCIC (pin 1) which is proportional to the sampled RF power.

The ASFIC contains a digital to analog converter (DAC) which provides a reference voltage of the control loop to the PCIC via R3517. The reference voltage level is programmable through the SPI line of the PCIC. This reference voltage is proportional to the desired power setting of the transmitter, and is factory programmed at several points across the frequency range of the transmitter to offset frequency response variations of the transmitter's power detector circuitry.

The PCIC provides a DC output voltage at pin 4 (INT) which is amplified and shifted in DC level by stages Q3501 and Q3502. The 0 to 4 volt DC range at pin 4 of U3501 is translated to a 0 to 8.5 volt DC range at the output of Q3501, and applied as VCONT to the power-adjust input pin of the first transmitter stage U3401. This adjusts the transmitter power output to the intended value. Variations in forward or reflected transmitter power cause the DC voltage at pin 1 to change, and the PCIC adjusts the control voltage above or below its nominal value to raise or lower output power.

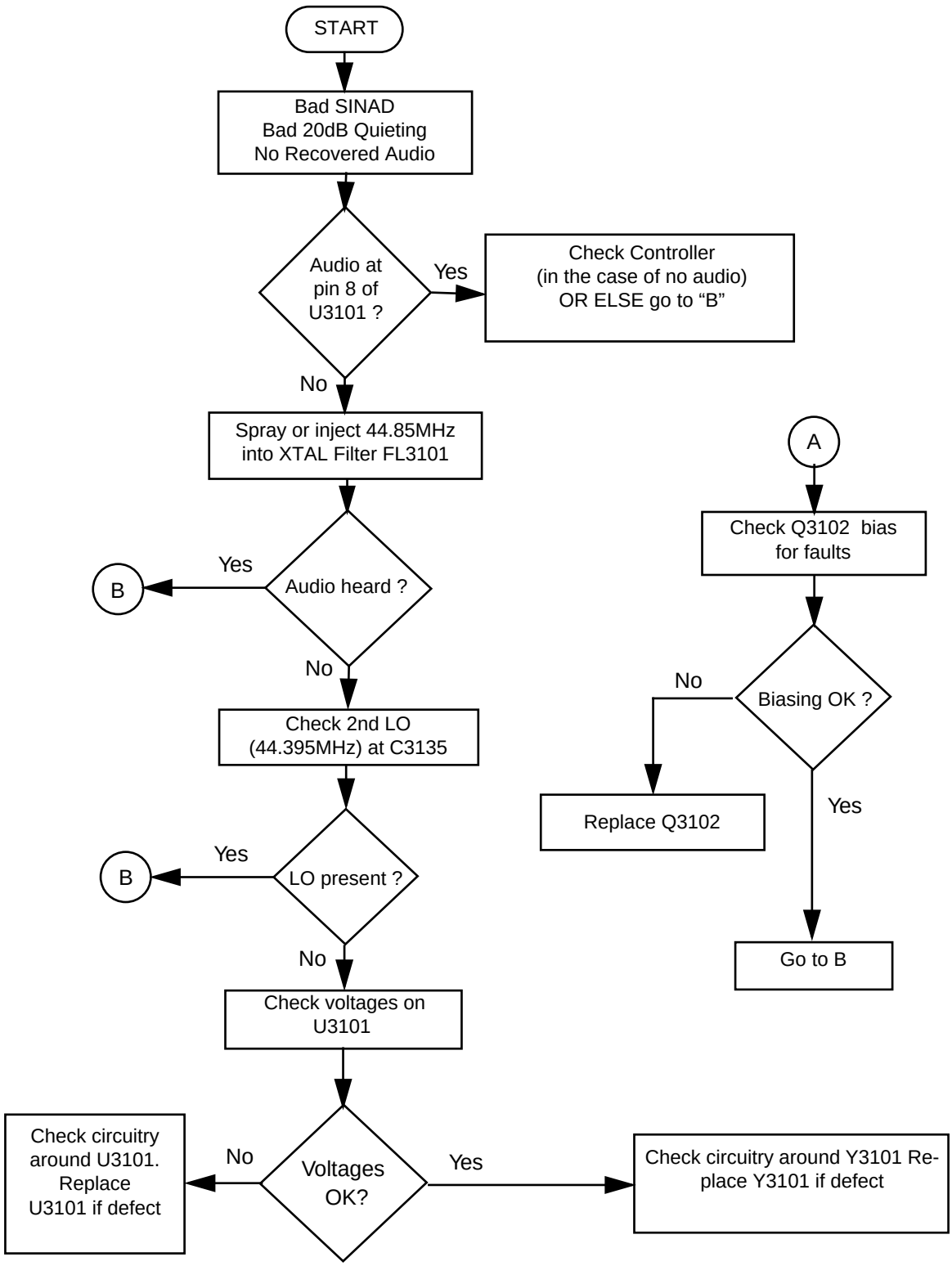
Capacitors C3502-4, in conjunction with resistors and integrators within the PCIC, control the transmitter power-rise (key-up) and power-decay (de-key) characteristic to minimize splatter into adjacent channels.

U3502 is a temperature-sensing device, which monitors the circuit board temperature in the vicinity of the transmitter driver and final devices, and provides a dc voltage to the PCIC (TEMP, pin 29) proportional to temperature. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

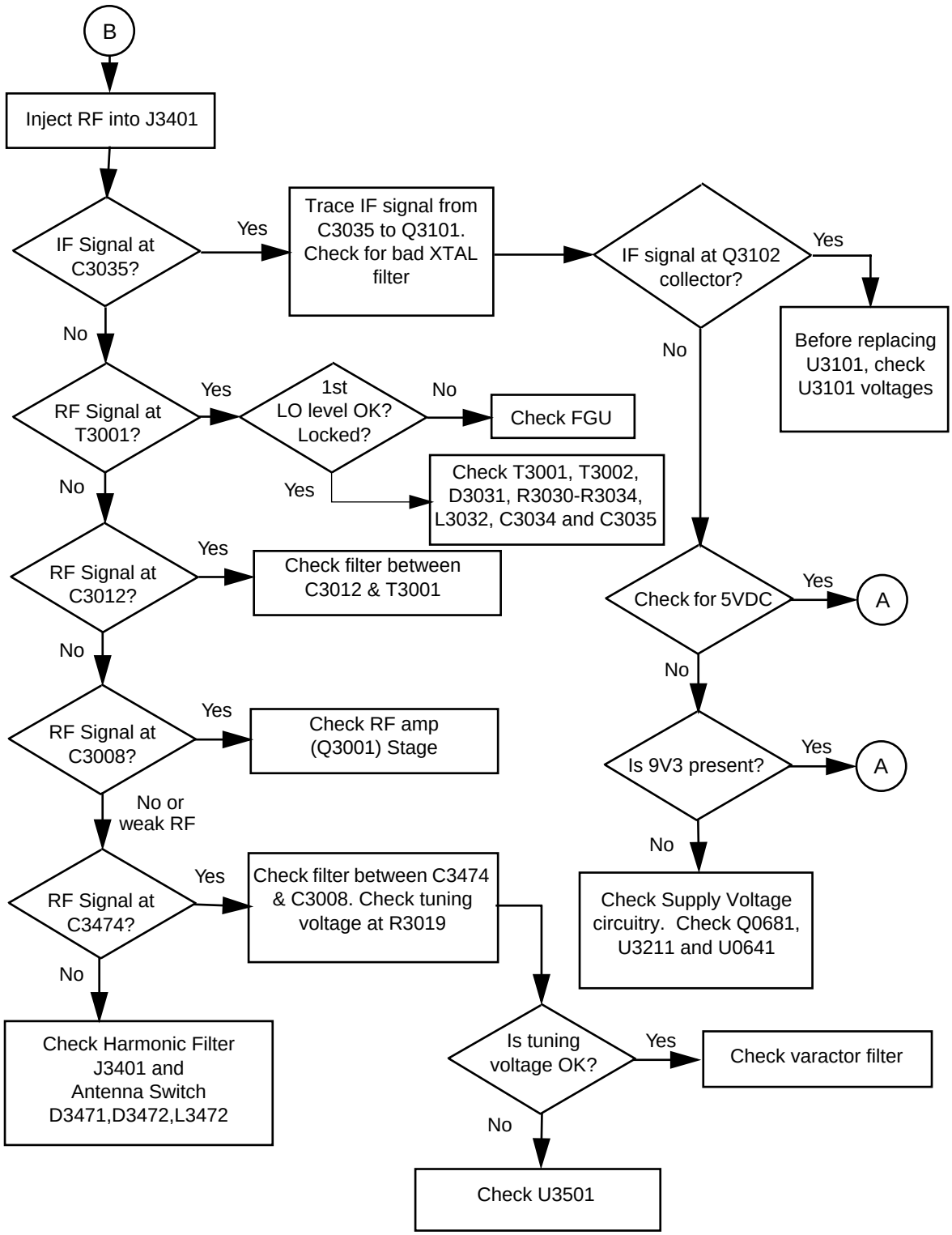
Chapter 3

TROUBLESHOOTING CHARTS

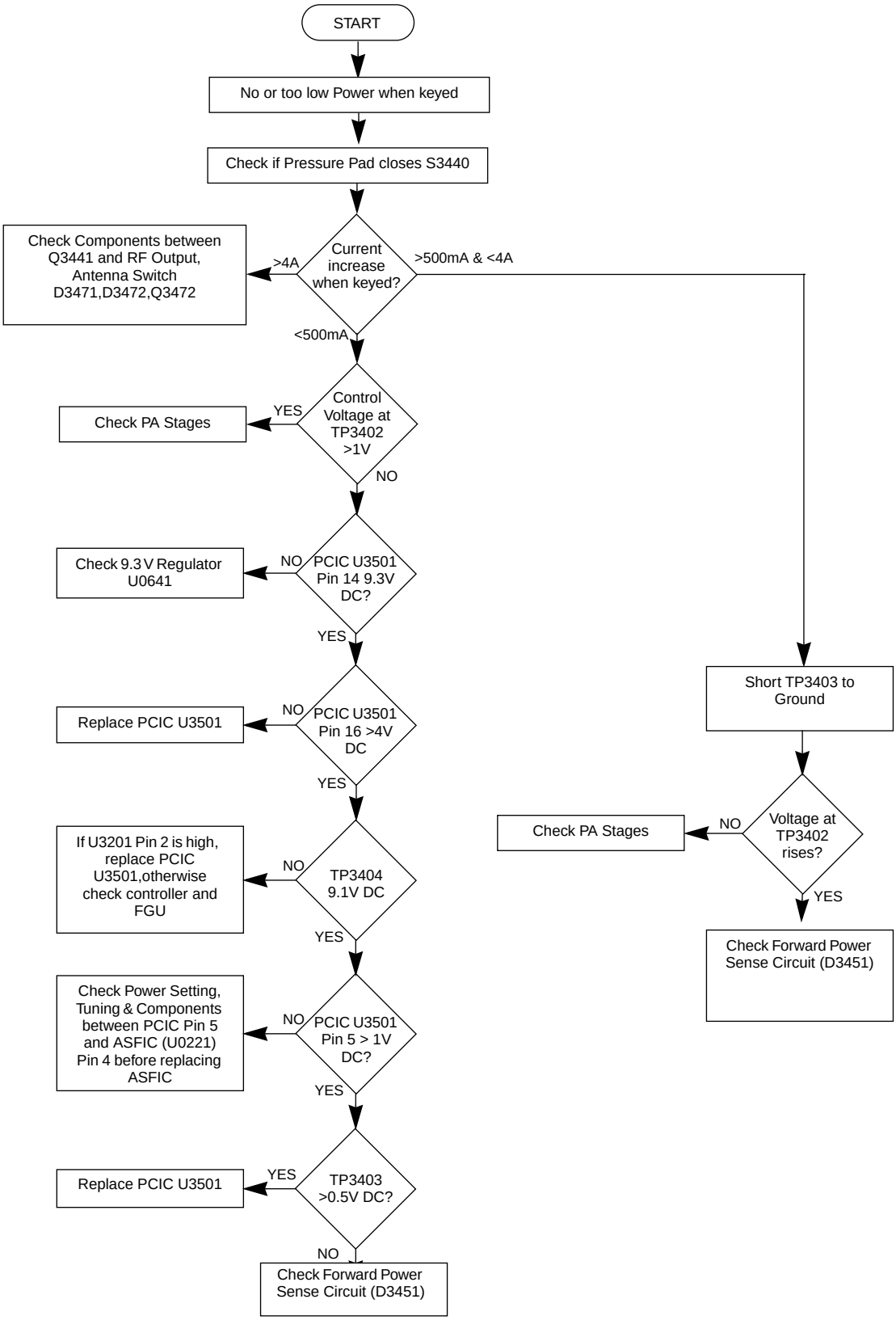
1.0 Troubleshooting Flow Chart for Receiver (Sheet 1 of 2)



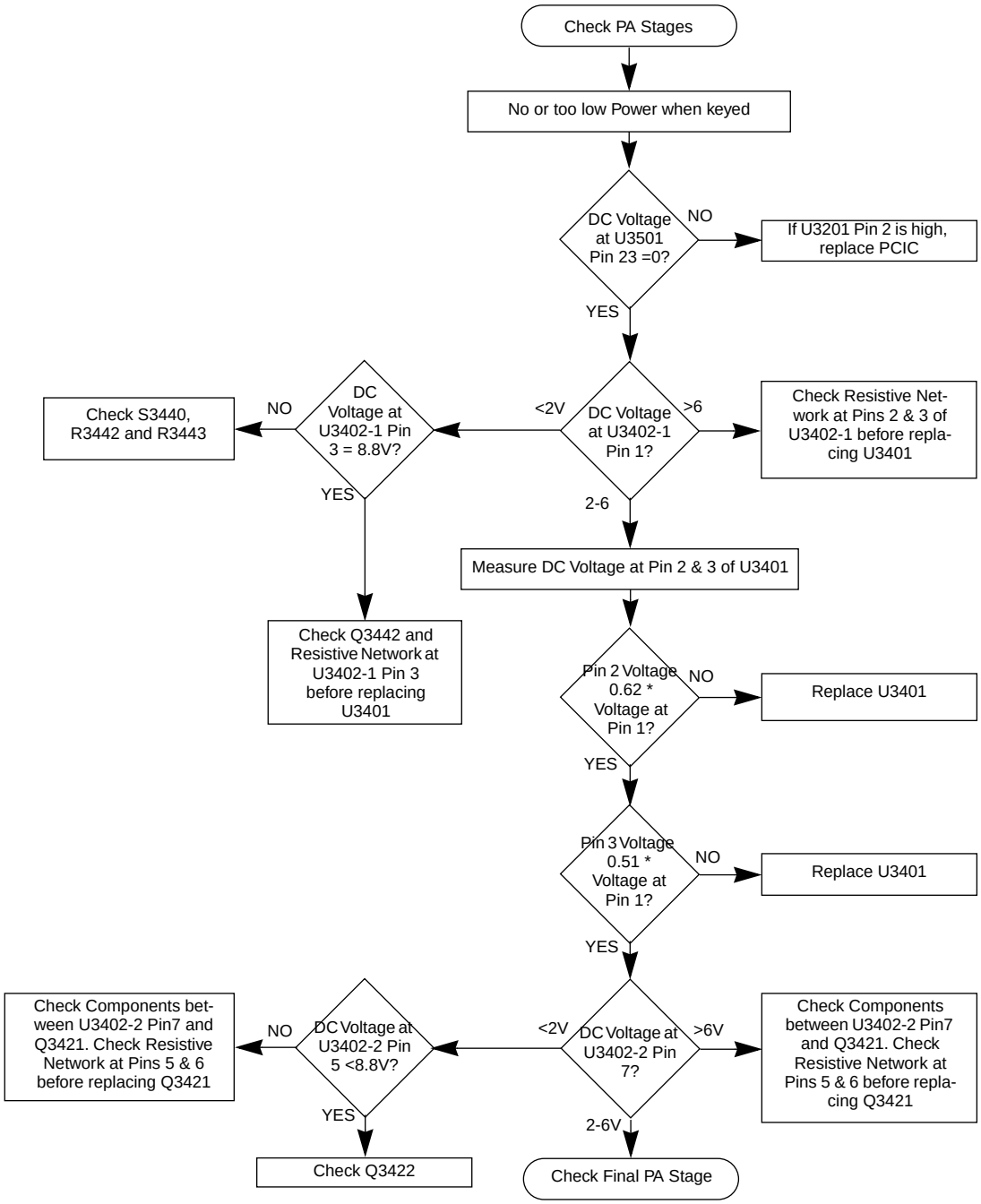
1.1 Troubleshooting Flow Chart for Receiver (Sheet 2 of 2)



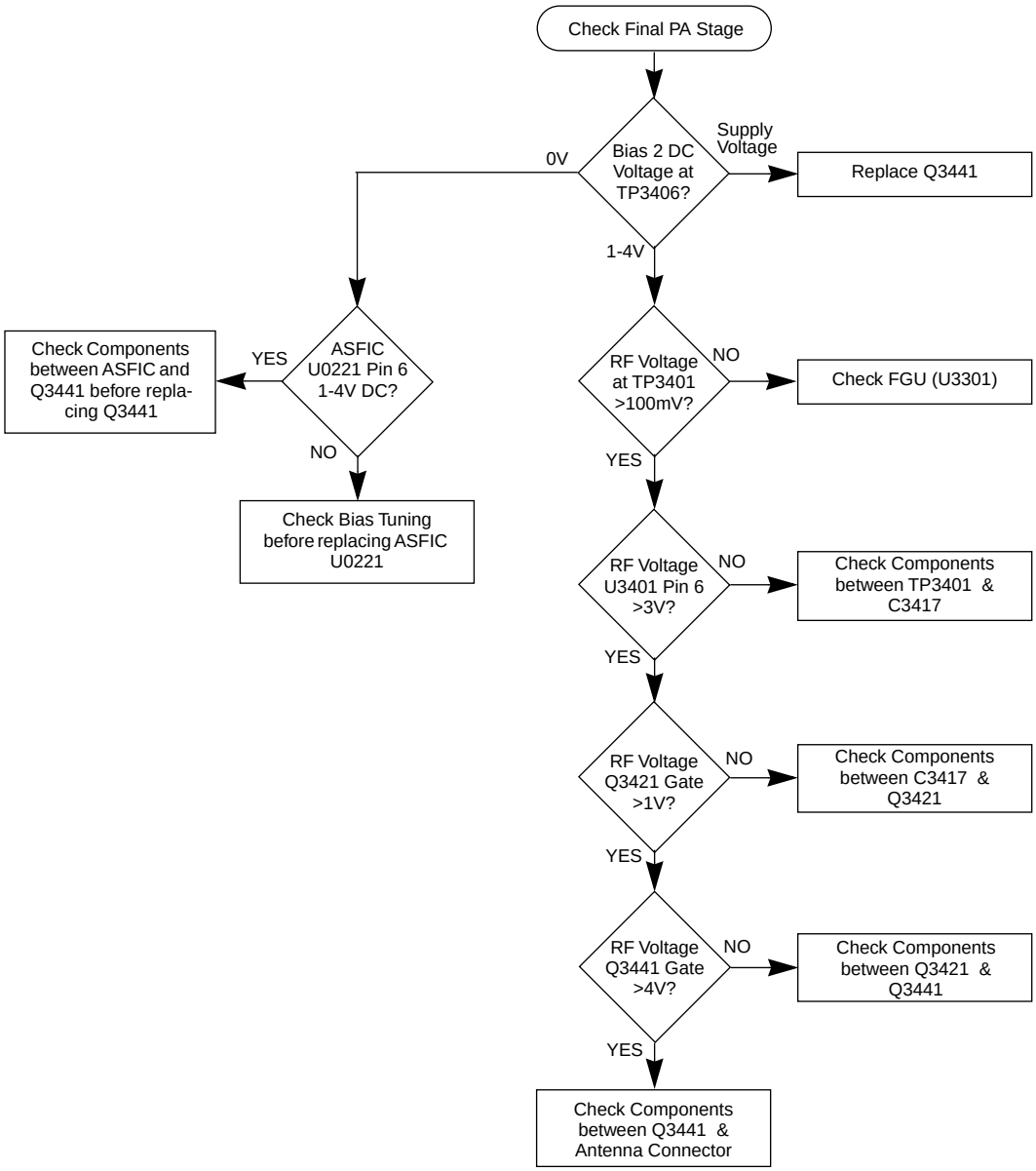
2.0 Troubleshooting Flow Chart for 25W Transmitter (Sheet 1 of 3)



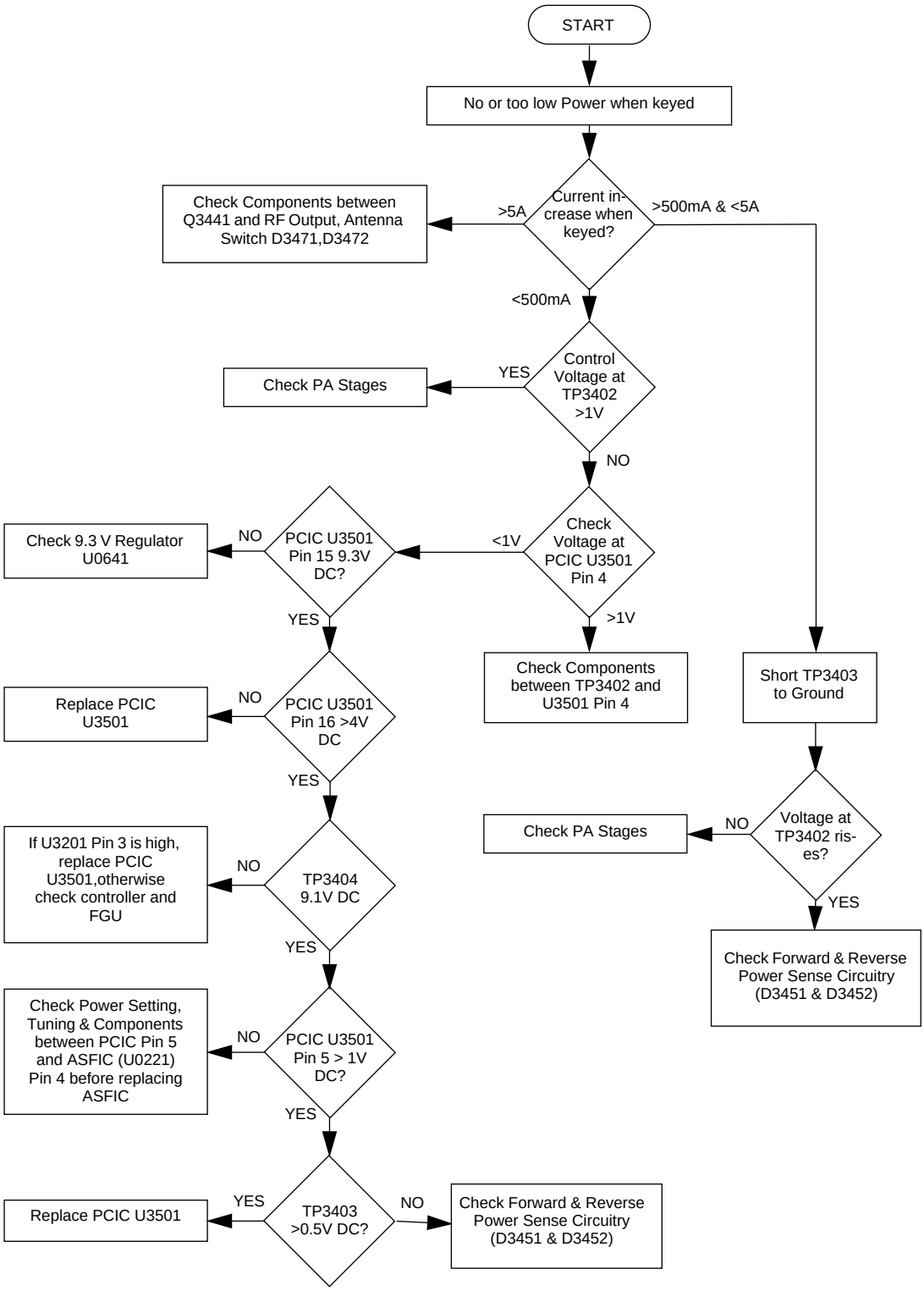
2.1 Troubleshooting Flow Chart for 25W Transmitter (Sheet 2 of 3)



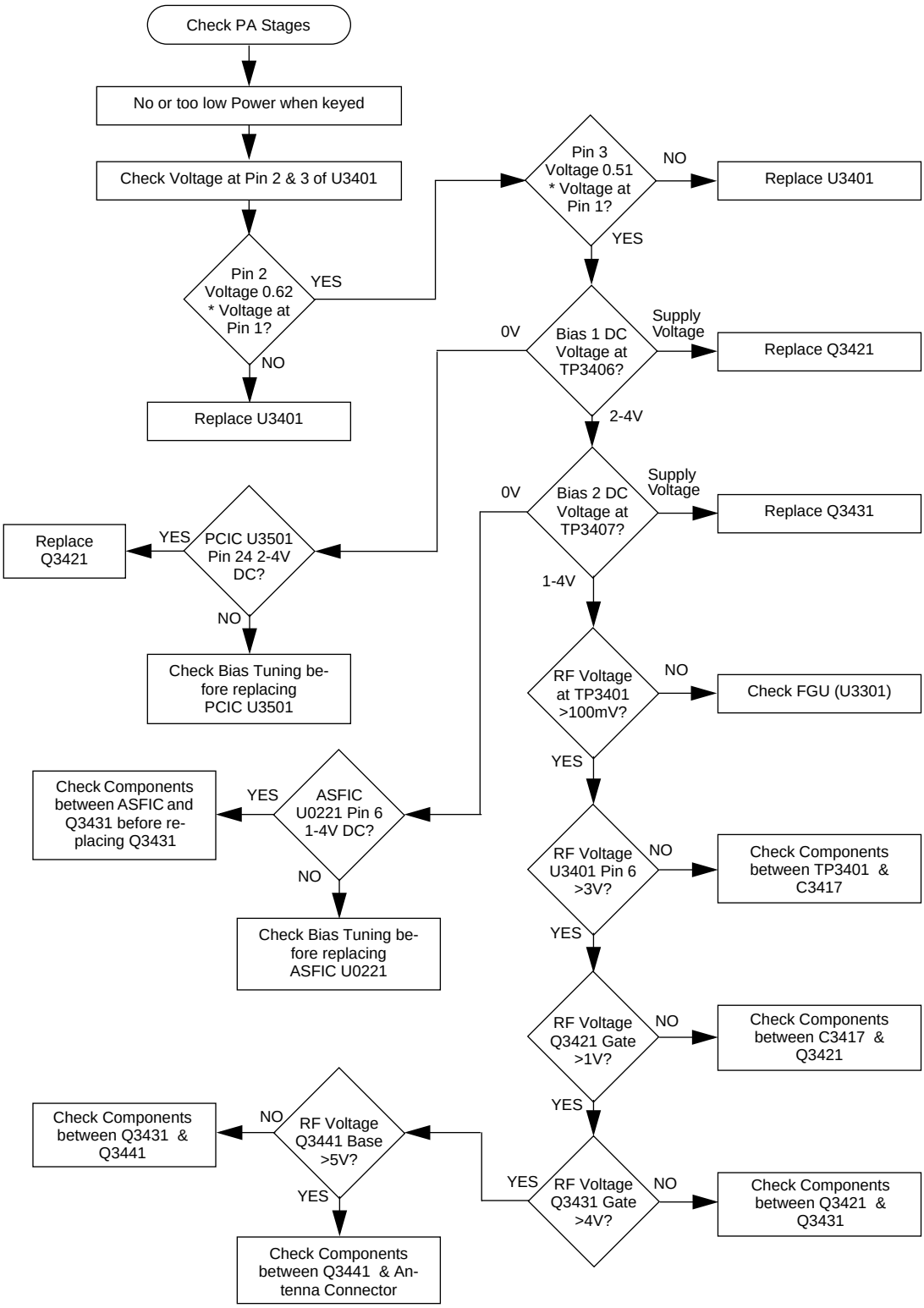
2.2 Troubleshooting Flow Chart for 25W Transmitter (Sheet 3 of 3)



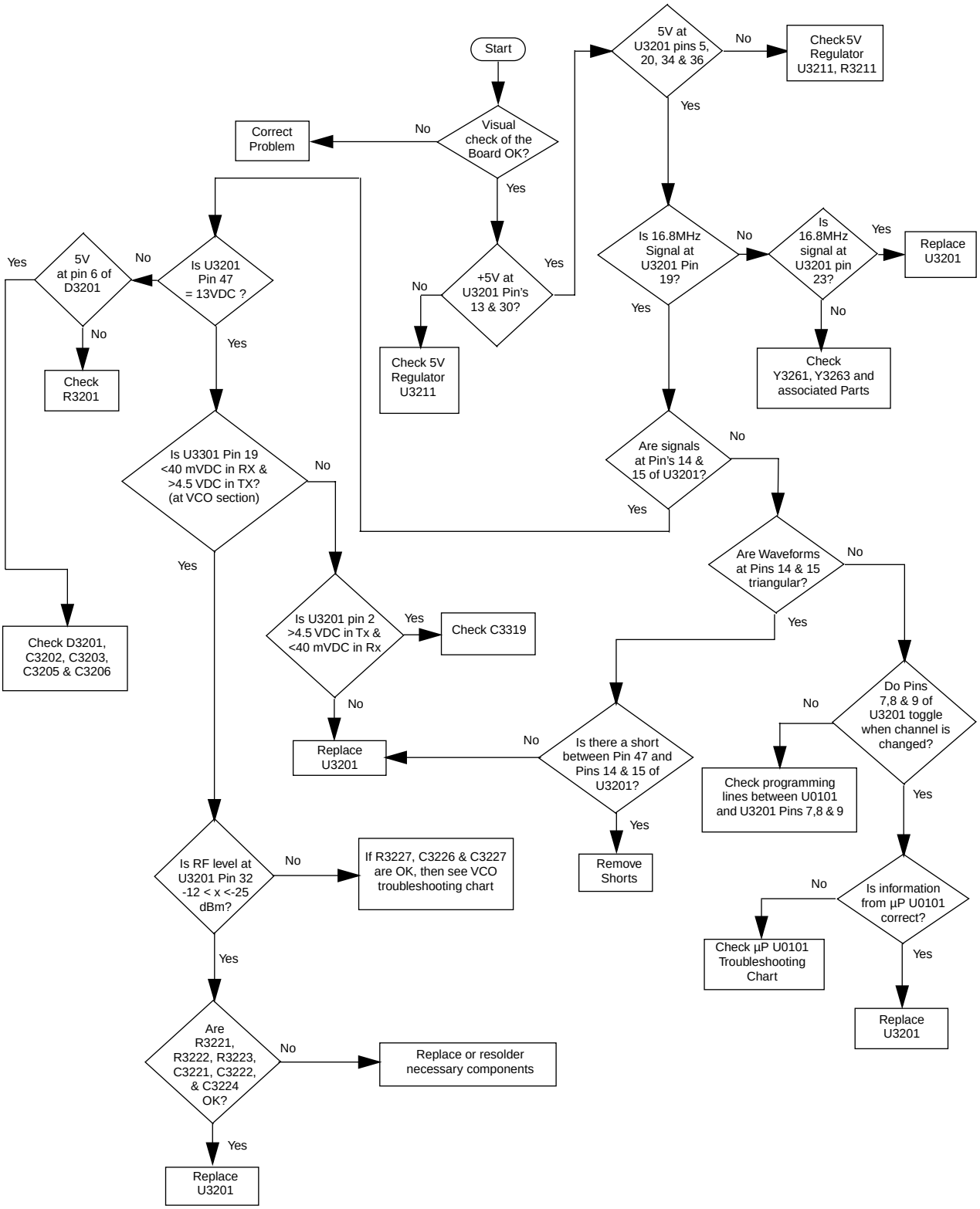
3.0 Troubleshooting Flow Chart for 45W Transmitter (Sheet 1 of 2)



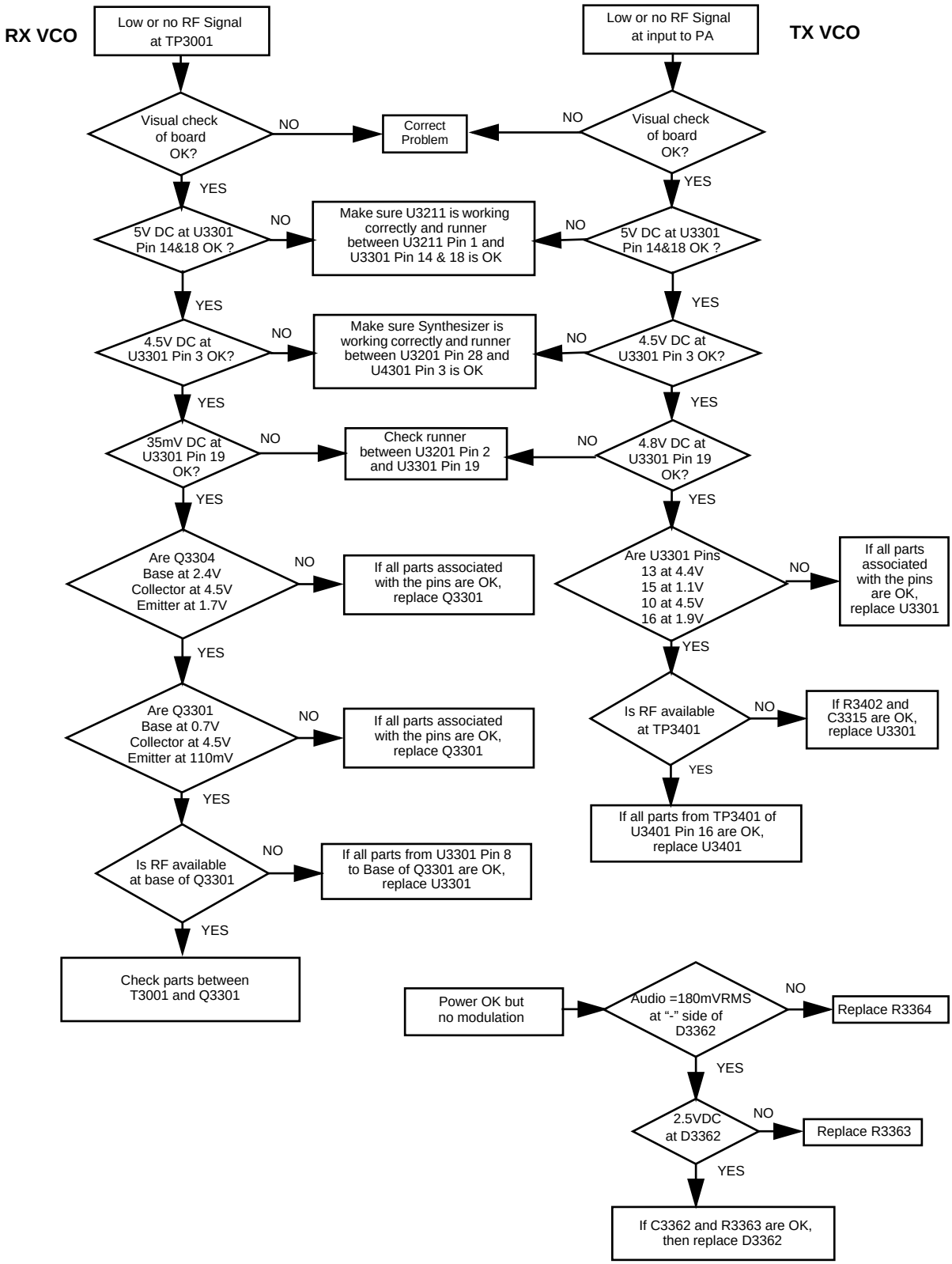
3.1 Troubleshooting Flow Chart for Transmitter (Sheet 2 of 2)



4.0 Troubleshooting Flow Chart for Synthesizer



5.0 Troubleshooting Flow Chart for VCO



Chapter 4

VHF PCB/SCHEMATICS/PARTS LISTS

1.0 Allocation of Schematics and Circuit Boards

1.1 Controller Circuits

The VHF circuits are contained on the printed circuit board (PCB) which also contains the Controller circuits. This Chapter shows the schematics for the VHF circuits only, refer to the Controller section for details of the related Controller circuits . The PCB component layouts and the Parts Lists in this Chapter show both the Controller and VHF circuit components. The VHF schematics and the related PCB and parts list are shown in the tables below.

Table 4-1 VHF 1-25W Diagrams and Parts Lists

Table 4-2 VHF 1-25W Diagrams and Parts Lists

Table 4-3 VHF 1-25W Diagrams and Parts Lists

Table 4-4 VHF 25-45W Diagrams and Parts Lists